TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. BUR920030092US1

In Re Application Of: **Allen et al**

Serial No.	Filing Date	Examiner	Group Art Unit
10/604,987	**08/28/2003**	**Unknown**	**Unknown**

Title: **The Use of a Layout-Optimization Tool to Increase the Yield and Reliability of VLSI Designs**

Address to:
Assistant Commissioner for Patents
Washington, D.C. 20231

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☐ the fee set forth in 37 CFR 1.17(p).

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10/604,987	08/28/2003	Unknown	Unknown

The Use of a Layout-Optimization Tool to Increase the Yield and Reliability of VLSI Designs

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

☐ A check in the amount of is attached.

☒ The Assistant Commissioner is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of
- ☒ Credit any overpayment.
- ☒ Charge any additional fee required.

Certificate of Transmission by Facsimile*

I certify that this document and authorization to charge deposit account is being facsimile transmitted to the United States Patent and Trademark Office (F

_____
(Date)

Signature

Typed or Printed Name of Person Signing Certificate

Certificate of Mailing by First Class Mail

I certify that this document and fee is being deposited 09/08/03 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the ~~Assistant~~ Commissioner for Patents, ~~Washington, D.C. 20231~~ Alexandria, VA 22313.

Signature of Person Mailing Correspondence

C. MUELLER

Typed or Printed Name of Person Mailing Certificate

***This certificate may only be used if paying by deposit account.**

Signature

Dated: Sept. 9, 2003

Richard M. Kotulak, Reg. No. 27,712
IP Law Department, Mail Stop 972E
IBM Corporation
1000 River Street
Essex Junction, VT 05452
Telephone: 802-769-4457

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Allen et al.

Serial No.: ~~Not Yet Assigned~~ 10/604,987 Group Art Unit: Not Yet Assigned

Filing Date: ~~Concurrently Herewith~~ 08/28/2003 Examiner: Unknown

For: THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE YIELD AND RELIABILITY OF VLSI DESIGNS

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

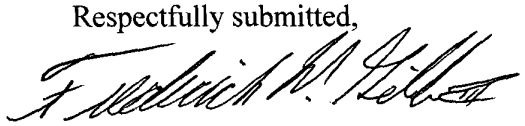
Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicants' duty of disclosure under 37 CFR §1.56, applicants respectfully bring the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,



Frederick W. Gibb, III
Registration No. 37,629

McGinn & Gibb, PLLC
2568-A Riva Road, Suite 304
Annapolis, Maryland 21401
(301) 261-8071
Customer No. 29154

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
BUR920030092US1	Not Yet Assigned
FILING	GROUP
Concurrently Herewith	Unknown

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		DE3326427	02/13/85	Germany				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			Allan et al., "Automated Redundant Via Placement for Increased Yield and Reliability", Proceedings of the SPIE - The International Society for Optical Engineering Conference, vol. 3216, 1997, pp. 114-125.
			Frank et al., "Yield Improvement of Wafer-Scale Integrated Systolic Structures Via Redundancy", 16th Annual IEEE Electronics and Aerospace Systems Conference and Exposition. 1983, pp. 317-322.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			IBM Technical Disclosure, "Yield and Reliability Enhancement Via Redundancy for VLSI Chips and Wafers," vol. 28, No. 1, 1985, pp. 36-42.
			Chen et al., "Layout Techniques for VLSI Yield Enhancement", Proceedings of the SPIE - The International Society for Optical Engineering Conference", vol. 4600, 2001, pp. 140-147.

EXAMINER	DATE CONSIDERED

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